What is claimed is:

1. A semiconductor device, comprising:

a semiconductor chip which has a circuit region defined in the central part thereof and a wiring region which surrounds the circuit region;

an integrated circuit which is formed on the circuit region;

a plurality of electrode pads which are formed on the circuit region and which are connected to the integrated circuit;

a plurality of first external terminals which are arranged over the circuit region;

a plurality of second external terminals which are arranged over the wiring region;

a first redistribution wiring which connects the electrode pad to the first external terminal;

a second redistribution wiring which connects the electrode pad to the second external terminal; and

a sealing film which covers over the circuit region and the wiring region such that the first and second external terminals are exposed from the sealing film.

2. The semiconductor device according to claim 1, further comprising a passive element which is provided on the wiring region and which regulates the electrical characteristics of the second redistribution wiring.

3. The semiconductor device according to claim 2, wherein the passive element includes a capacitor.

4. The semiconductor device according to claim 2, wherein the passive element includes a plurality of capacitors which are standardized so as to have the same size.

5. The semiconductor device according to claim 2, wherein the passive element includes an inductor.

6. The semiconductor device according to claim 2, wherein the passive element includes a plurality of inductors which are standardized so as to have the same size.

7. The semiconductor device according to claim 2, wherein the passive element has a plurality of passive elements which are arranged in the form of an array in the wiring region.

8. The semiconductor device according to claim 2, wherein the passive element is formed in a layer in which the second redistribution rewiring is formed.

9. The semiconductor device according to claim 2, wherein the passive element is formed in a layer that lies beneath a layer in which the second redistribution wiring is formed.

10. The semiconductor device according to claim 2, wherein the second redistribution wiring comprises a wiring part that connects the electrode pad to the passive element and another wiring part that connects the passive element the second external terminal.

11. The semiconductor device according to claim 10, further comprising a passive element electrode pad, in which the passive element is connected to the wiring part via the passive element electrode pad.

12. The semiconductor device according to claim 1, wherein

the electrode pad has a plurality of electrode pads which are arranged along the boundary between the circuit region and the wiring region.

13. The semiconductor device according to claim 1, further comprising a first post electrode having a top surface and a bottom surface, wherein the first external terminal is provided on the top surface and the first redistribution wiring is connected to the bottom surface.

14. The semiconductor device according to claim 1, further comprising a second post electrode having a top surface and a bottom surface, wherein the second external terminal is provided on the top surface and the second redistribution wiring is connected to the bottom surface.

15. A semiconductor device, comprising:

a semiconductor substrate which has a first region that is provided with a plurality of circuit element connection pads, and a second region that surrounds the first region;

a plurality of first external terminals which are arranged on the first region;

a plurality of second external terminals which are arranged on the second region;

a plurality of first wiring structures which are formed on the first region, and electrically and individually connecting a plurality of the first external terminals and a first predetermined number of the circuit element connection pads;

a plurality of second wiring structures which are

formed ranging from the first region to the second region, and electrically and individually connecting a plurality of the second external terminals and a second predetermined number of the circuit element connection pads;

a passive element which is electrically connected to one of the second wiring structures.

16. The semiconductor device according to claim 15, wherein;

each of the first wiring structures contains a first redistribution wiring layer which is electrically and individually connected to one of the first predetermined number of the circuit element connection pads, and a first post electrode which electrically and individually connects the first redistribution wiring layer and the one of the first external terminals;

each of the second wiring structures contains a second redistribution wiring layer which is formed ranging from the first region to the second region and is electrically and individually connected to one of the circuit element connection pads, and a second post electrode which electrically and individually connects the second redistribution wiring layer and one of the second external terminals; and

the passive element is electrically connected to one of the second redistribution wiring layer.

17. The semiconductor device according to claim 16, wherein;

the passive element is a capacitor which has an upper

electrode, a lower electrode and a dielectric film which is placed between the upper electrode and the lower electrode; and

the upper electrode is electrically connected to one of the second redistribution wiring layer, and the lower electrode is electrically connected to another of the second redistribution wiring layer.

18. The semiconductor device according to claim 16, wherein the passive element is a inductor which is placed in a route of the second redistribution wiring layer.

19. The semiconductor device according to claim 15, wherein;

each of the first wiring structures contains a first redistribution wiring layer which is electrically and individually connected to one of the first predetermined number of the circuit element connection pads, and a first post electrode which electrically and individually connects the first redistribution wiring layer and the one of the first external terminals;

each of the second wiring structures contains a second redistribution wiring layer which is formed ranging from the first region to the second region and is electrically and individually connected to one of the circuit element connection pads, and a second post electrode which electrically and individually connects the second redistribution wiring layer and one of the second external terminals; and

the passive element is electrically connected to one of the second redistribution wiring layer via a passive element

electrode pad which is placed over the second region.

20. The semiconductor device according to claim 19, wherein;

the passive element is a capacitor which has an upper electrode, a lower electrode and a dielectric film which is placed between the upper electrode and the lower electrode;

a first capacitor connection pad which is a passive element electrode pad being electrically connected to the upper electrode, and a second capacitor connection pad which is a passive element electrode pad being electrically connected to the lower electrode are comprised; and

the first capacitor connection pad is electrically connected to one of the second redistribution wiring layer, and the second capacitor connection pad is electrically connected to another of the second redistribution wiring layer.

21. The semiconductor device according to claim 19, wherein;

the passive element is a inductor,

two passive element electrode pads are electrically connected to one passive element, in which these two passive element electrode pads are first and second inductor connection pads; and

the first and second inductor connection pads are electrically connected to corresponding second redistribution wiring layer respectively.

22. The semiconductor device according to claim 19, wherein a plurality of the passive elements are arranged in the shape of an array.